## AMENDMENTS TO THE CLAIMS:

As set forth in the **Listing of Claims** section of this paper, Applicants hereby amend claim 6 and cancel claims 1-5, 7-12, 18, 26, 29 and 32-50, without prejudice or disclaimer of the subject matter therein.

## COMPLETE LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-5. (Cancelled)

6. (Currently Amended) A high-density circuit module comprising:

a first CSP having an upper and a lower major surface and a set of CSP contacts along the lower major surface;

a second CSP having first and second lateral edges and upper and lower major surfaces and a set of CSP contacts along the lower major surface, the first and second lateral edges delineating an extent of the upper major surface of the second CSP;

a form standard disposed above the upper surface of the second CSP, the form standard defining a standard sized form; and

a flex circuit that is at least partially disposed about the form standard.

7.-12. (Cancelled)

13. (Original) A memory access system comprising:

a memory expansion board;

a high-density circuit module devised in accordance with claim 6, the high-density circuit module being mounted on the memory expansion board;

a switching multiplexer mounted on the memory expansion board, the switching multiplexer for switching data lines between the first and second integrated circuits; and

a decode logic circuit for decoding chip selection signals from a control circuit and providing a switching multiplexer control signal.

14. (Original) A memory access system comprising:

a high-density circuit module devised in accordance with claim 6;

a switch for connecting a datapath to one of the plural integrated circuits of the high-density circuit module;

a decode logic for generating a control signal that causes the switch to connect the datapath to one of the plural integrated circuits in response to a combination signal comprised of a clock signal and a chip select signal.

15. (Original) The memory access system of claim 14 in which the plural integrated circuits of the high-density circuit module number four.

16. (Original) A memory access system comprising:

plural memory expansion boards each populated with plural high-density circuit modules, each of which plural high-density circuit modules being devised in accordance with claim 6;

plural multiplexers mounted upon each of the plural memory expansion boards, the plural multiplexers for making connections between a datapath and single ones of the plural integrated circuits comprising the high-density circuit modules;

decode logic on each of the plural memory expansion boards, the decode logic for generating a control signal in response to a combination signal comprised of a clock signal and a chip select signal, the control signal causing at least one of the plural multiplexers to connect a particular datapath to a particular one of the plural integrated circuits.

17. (Original) The memory access system of claim 16 in which the multiplexers are FET multiplexers.

18. (Cancelled)

19. (Original) The memory access system of claim 16 in which the plural high-density circuit modules are comprised of four integrated circuits.

20. (Original) The memory access system of claim 16 in which the plural high-density circuit modules are comprised from two integrated circuits.

21. (Original) A memory access system comprising:

a memory board having a board memory signal data connection that provides a connection for memory signals between a plurality of integrated circuits mounted on the memory board and memory control circuitry;

a high-density circuit module comprised of first, second, third, and fourth individual integrated circuits, the high-density circuit module being mounted on the memory board and devised in accordance with claim 6;

a switching multiplexer mounted on the memory board, the switching multiplexer having a set of plural input data connections, individual ones of the plural input data connections connected to provide individual data connections between each of the first, second, third, and fourth individual integrated circuits and the switching multiplexer; and

a decode logic circuit for decoding chip selection signals from a control circuit and providing a switching multiplexer control signal.

22. (Original) The memory access system of claim 21 in which the switching multiplexer further comprises an output data connection connected to the board signal memory data connection.

23. (Original) The memory access system of claim 22 in which the switching multiplexer provides selective individual connection between the board signal memory data connection and the first, second, third, and fourth individual integrated circuits.

24. (Original) The memory access system of claim 23 in which the individual connection between the board signal memory data connection and the first, second, third, and fourth individual integrated circuits occurs in response to the switching multiplexer control signal from the decode logic circuit.

25. (Original) The memory access system of claim 21 in which the decode logic circuit is mounted on the memory board.

26. (Cancelled)

27. (Original) A memory access system comprising:

X memory expansion boards each populated with Y high-density circuit modules devised in accordance with claim 6, each of which Y high-density circuit modules being comprised of Z individual integrated circuits;

plural multiplexers mounted upon each of the X memory expansion boards, the plural multiplexers each for selectively making connections between a datapath and single ones of the Z integrated circuits comprising each of the Y high-density circuit modules;

decode logic on each of the plural memory expansion boards, the decode logic for generating a control signal in response to a combination signal comprised of a clock signal and a chip select signal, the control signal causing at least one of the plural multiplexers to connect a particular datapath to a particular one of the Z integrated circuits.

28. (Original) The memory access system of claim 27 in which the multiplexers are FET multiplexers.

29. (Cancelled)

30. (Original) The memory access system of claim 27 in which Z equals 4.

31. (Original) The memory access system of claim 27 in which Z equals 2.

32.-50. (Cancelled)